CLAIMS

What is claimed is:

1. A register file comprising:

   a multi-level multiplexer output circuit coupled to a global bit trace;

   keeper circuitry coupled to said global bit trace and a driving signal trace; and

   decoder circuitry coupled to said keeper circuitry to selectively decouple the driving signal trace from said global bit trace.

2. The register file of claim 1 wherein said multi-level multiplexer output circuit comprises a plurality of local bit traces.

3. The register file of claim 2 further comprising a plurality of select signal traces corresponding to said plurality of local bit traces and wherein said decoder circuitry is designed to:

   determine whether one of said plurality of local bit traces evaluates;

   determine if one of said plurality of select signal traces, corresponding to the evaluated bit trace, is asserted; and

   conditionally decouple said driving signal trace from said global bit trace, based at least in part on the results of said determines.

4. The register file of claim 3 wherein said conditionally decoupling occurs upon determining one of said plurality of local bit traces evaluates and determining one of said plurality of select signal traces, corresponding to said evaluated bit trace, is asserted.

5. The register file of claim 3 wherein said decoder is designed to perform said determining if one of said plurality of local bit traces evaluates by determining whether one of a plurality of row select signals and one of a plurality of data output signals couples one of said plurality of local bit traces to a first supply node.

6. The register file of claim 3 wherein said keeper circuitry comprises a P-type MOS transistor with a source coupled to said driving signal trace and a drain coupled to said global bit trace, and said selective decoupling of said driving signal trace from said global bit trace comprises turning off said P-type MOS transistor.

7. The register file of claim 2 wherein said local bit traces are coupled to a supply node through corresponding local bit trace precharge circuitries.

8. The register file of claim 7 wherein said local bit trace precharge circuitries comprise a P-type MOS transistor and an N-type MOS transistor, wherein a drain of said P-type MOS transistor is coupled to a power supply trace and a source of said P-type MOS transistor is coupled to a drain of said N-type MOS transistor and wherein a drain of said N-type MOS transistor is coupled to a corresponding local bit trace.

9. The register file of claim 8 wherein a gate of said P-type MOS transistor is coupled to a clock line and a gate of said N-type MOS transistor is coupled to said power supply trace.

10. The register file of claim 1 wherein said keeper circuitry comprises a weak P-type MOS transistor.

11. The register file of claim 1 further comprising a precharge transistor to precharge said global bit trace.

12. The register file of claim 1 wherein said multi-level multiplexer output circuit comprises a 3-stack pulldown.

13. The register file of claim 1 wherein said multi-level multiplexer output circuit comprises a plurality of low threshold voltage transistors.

14. A method comprising:

determining if one of a plurality of local bit traces evaluates;

determining if one of a plurality of select signals on select signal traces, corresponding to local bit traces, is asserted; and

conditionally decoupling a driving signal trace from a global bit trace, based at least in part on the results of said determining operations.

15. The method of claim 14 wherein said conditionally decoupling occurs upon determining one of said plurality of local bit traces evaluates and determining one of said plurality of select signal traces, corresponding to said evaluated bit trace, is asserted.

16. The method of claim 14 wherein said determining if one of a plurality of local bit traces evaluates comprises determining whether one of a plurality of row select signals and one of a plurality of data output signals couples one of said plurality of local bit traces to a first supply node.

17. The method of claim 14 wherein said conditionally decoupling a driving signal trace from a global bit trace comprises turning off a switching element.

18. The method of claim 17 wherein said switching element is a weak P-type MOS device.

19. A system comprising:

a processor having:

a register file output signal trace,

a driving signal trace, and

a register file including

a global bit trace coupled to said register file output signal trace;

a multi-level multiplexer output circuit coupled to said global bit trace,

keeper circuitry coupled to said global bit trace and the driving signal trace, and

decoder circuitry coupled to said keeper circuitry to selectively decouple the driving signal trace from said global bit trace;

a memory configured to store data; and

a bus coupled to the processor and memory to facilitate data exchange between the processor and memory.

20. The system of claim 19 wherein said multi-level multiplexer output circuit comprises a plurality of local bit traces.

21. The system of claim 20 wherein said register file further comprises a plurality of select signal traces corresponding to said plurality of local bit traces and wherein said decoder circuitry operates to:

determine whether one of said plurality of local bit traces evaluates;

determine whether one of said plurality of select signal traces,

corresponding to said evaluated bit trace, is asserted; and

conditionally decouple said driving signal trace from said global bit trace,

based at least in part on the results of said determined operations.

22. The system of claim 21 wherein said conditionally decoupling occurs upon determining one of said plurality of local bit traces evaluates and determining one of said plurality of select signal traces, corresponding to said evaluated bit trace, is asserted.

23. The system of claim 21 wherein said determining if one of said plurality of local bit traces evaluates comprises determining whether one of a plurality of row select signals and data output signals couples said local bit trace to a first supply node.

24. The system of claim 21 wherein said keeper circuitry comprises a P-type MOS transistor with a source coupled to said driving signal trace and a drain coupled to said global bit trace and wherein said intelligent decoupling said driving signal trace from said global bit trace comprises turning off said P-type MOS transistor.

25. The system of claim 19 wherein said keeper circuitry comprises an upsized P-type MOS transistor.

26. The system of claim 19 wherein said multi-level multiplexer output circuit comprises a plurality of low threshold voltage transistors.

27. The system of claim 19 wherein the system further comprises a graphic controller coupled to the bus.